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EXAMINER	
VITAL, PIERRE M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,874	CHANG ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 2, 2006 has been entered.

Information Disclosure Statement

2. The information disclosure statement (IDS) filed February 2, 2006 complies with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

3. This Office Action is in response to applicant's communication filed February 2, 2006 in response to PTO Office Action mailed October 31, 2005. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

4. In response to the last Office Action, no claims have been amended. No claims have been canceled. No claims have been added. As a result, claims 1-35 remain pending in this application.

Response to Arguments

5. Applicant's arguments, see Remarks, filed August 1, 2005, with respect to the rejection(s)of claim(s) 1-35 have been fully considered and they are not persuasive. Therefore, the rejection has been maintained and reiterated below for applicant's convenience.

As to the Remarks, Applicant asserted that:

(a) The non-volatile storage device of MacDonald is not equivalent to the AFSD of claim 1 since there is no disclosure within MacDonald teaching storing user applications and data files on non-volatile storage device (NVSD) 7 of MacDonald.

It is to be noted that on page 2, MacDonald discloses "Although the non-volatile storage device is preferably a Non-volatile Memory (NVM), which is preferably coupled to the DMAC, it could alternatively be a hard file, such as a disc, CD or optical CD, or other storage medium, such as magnetic tape". It is further noted that the non-volatile storage of MacDonald contains similarities with the application and file storage device claimed by applicant, such as being a CD or optical disk or other type of storage devices.

Furthermore, Applicant argues that there is no disclosure within MacDonald teaching storing user applications and data files on non-volatile storage device (NVSD) 7 of MacDonald. In response to applicant's argument that the references fail to show

certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., user or general-purpose applications) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The non-volatile storage of MacDonald does store applications and data files. Applicant would be advised to amend the claims to clearly distinguish that the applications and data files are "user applications and data files".

(b) MacDonald does not teach that one or more of the files contain the Basic Input/Output System (BIOS).

MacDonald teaches that the data files include BIOS. It is to be noted that the BIOS is the initial operating code for initializing various hardware components as is well known in the art. Therefore, the person skilled in the art would consider the implementation of storing the BIOS in the non-volatile storage device without exercising of inventive activity.

Applicant's arguments regarding the independent claims attempt to show nonobviousness by attacking references individually where the rejections are based on combinations of references. The test for obviousness is what the combined teachings of

the references would have suggested to those of ordinary skill in the art. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981)., In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

6. Furthermore, upon further consideration, a new ground(s) of rejection is also made in view of Gibson et al (WO 01/52062) combined with other references. Rejection based on this new ground of rejection follows herewith.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 1-3, 6-9, 14, 16-18, 20, 22-24, 26-28 and 31-32 are rejected under 35 U.S.C. 102(a) as being anticipated by Gibson et al (WO 01/52062).

As per claim 1, Gibson discloses a system for starting operation of an intelligent device comprising:

an application and file storage device configured to read and write data files, one or more of the data files including the basic input/output system (BIOS) interface (page

2, lines 19-21; page 7, lines 27-31). It is to be noted that the BIOS is the initial operating code for initializing various hardware components (also described in page 1, lines 19-24 in the Background of the Invention, part of the description in the present application));

random access memory (RAM) (Fig. 1; RAM 16);

a loading logic circuit that copies a portion of the BIOS from the storage device into the RAM (page 2, lines 22-27).

As per claim 2, Gibson discloses the loading logic circuit is configured to copy the portion of the BIOS from the application and file storage device into the RAM without using a microprocessor (page 2, lines 22-28; page 7, lines 29-31).

As per claim 3, Gibson discloses the application and file storage device is a flash memory device (page 3, lines 30-33).

As per claim 6, Gibson discloses the loading logic circuit is contained in a programmable logic device (page 4, lines 6-7).

As per claim 7, Gibson discloses the circuit comprises board level components (page 4, lines 15-19).

As per claim 8, Gibson discloses the loading logic circuitry stores the BIOS at any location of the storage device (page 2, line 23; the subject matter of claim 8, is

implicitly disclosed in Gibson since no specific address for the storing of the bios in the storage device is disclosed. This implies that every address in the storage device is suitable for storing the BIOS).

As per claim 9, Gibson discloses the loading logic circuitry copies the BIOS to any location in the RAM (page 7, lines 29-31; the subject matter of claim 8, is implicitly disclosed in Gibson since no specific address for the storing of the bios in the storage device is disclosed. This implies that every address in the storage device is suitable for storing the BIOS).

As per claim 14, Gibson discloses a method of starting a smart device comprising:

resetting operation of a microprocessor (page 3, lines 26-29; page 4, lines 10-14); and thereafter

suspending operation of the microprocessor (page 4, lines 10-14); and thereafter

copying a portion of a BIOS from an application and file storage device into RAM (page 2, lines 22-26); and thereafter

starting operation of the microprocessor (page 2, lines 26-28).

As per claim 16, Gibson discloses reading the portion of the BIOS from the RAM with the central processing unit after the step of starting operation of the microprocessor (page 4, lines 35-37).

As per claim 17, Gibson discloses the step of copying the BIOS from a memory storage device into RAM is controlled by a state machine (page 4, linre15).

As per claim 18, Gibson discloses the state machine is implemented in an ASIC (Fig. 8; page 6, lines 34-36).

As per claim 20, Gibson discloses the application and file storage device is a flash memory device (page 3, lines 30-33).

Claim 22 is rejected using the same rationale as for the rejection of claims 1 and 2 above.

Claim 23 is rejected using the same rationale as for the rejection of claims 1 and 2 above.

As per claim 24, Gibson discloses the application and file storage device is a NAND flash memory device (page 3, lines 30-33).

Claim 26 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 27 is rejected using the same rationale as for the rejection of claim 7 above.

Claim 28 is rejected using the same rationale as for the rejection of claim 16 above.

Claim 31 is rejected using the same rationale as for the rejection of claims 1, 14 and 22 above.

As per claim 32, Gibson discloses the application and file storage device comprises a non-volatile solid-state memory device (page 2, lines 7-9).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 4, 15, 21, 25 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gibson et al (WO 01/52062) and Christeson et al (US 5,579,522).

As per claims 4, 21, 25 and 33, Gibson discloses the claimed invention as detailed above in the previous paragraphs. Gibson does not specifically teach that the

application and file storage device is a magnetic or optical disk drive as recited in the claim.

Christeson discloses a magnetic or optical disk drive as an application and file storage device for storing and updating non-volatile code and/or data without the need for removing and/or replacing any computer system hardware components (col. 4, lines 39-41; col. 2, lines 36-39).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the system of Gibson to include a magnetic or optical disk drive storage device because it was well known to benefit by storing information and instructions without the need for removing and/or replacing any computer system hardware components as taught by Christeson.

As per claim 15, Gibson discloses the claimed invention as detailed above in the previous paragraphs. Gibson does not specifically teach a user selecting which BIOS of multiple BIOS to copy into the RAM as recited in the claim.

Christeson discloses the following technical features: an additional BIOS region can be used to extend the system BIOS memory area. It can be seen that, the storage device can include multiple BIOSs and a user can select which BIOS to be copied into RAM (see col. 2, lines 41-55 of the description). Therefore, it is easy for

those skilled in the art to obtain the technical solution of claim 15 based on the above combination of references.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the system of Gibson to include additional BIOS regions because it was well known to allow the processing logic of the computer system to update or modify any selected block of memory without affecting the contents of other blocks (column 2, lines 46-49) as taught by Christeson.

11. Claims 5, 19 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gibson et al (WO 01/52062) and Klein (US 6,216,224).

As per claim 29, MacDonald and AAPA disclose the claimed invention as detailed above in the previous paragraphs. However, MacDonald and AAPA do not specifically teach the use of the address counter as recited in the claim.

Klein discloses a state machine drives the RSC to perform a number of operations that result in transfer of the ROM data to the RAM (equivalent to enabling the application and file storage device and the RAM); the address stored in the decrementing address counter 322 is used both to read data from the ROM and to write data to the RAM; the decrementing address counter 322 is decremented by one prior to

the start of the first bus cycle of the next RSC operation (see col. 5, line 51 to col. 6, line 27 of the description for details). It can be seen that, the address counter is enabled to output a value and the value is correlated with a RAM address; while Klein discloses decrementing the value of the address counter. However, incrementing or decrementing the value of a counter belongs to the common sense for those skilled in the art and the corresponding incrementing or decrementing operation can be performed according to need.

Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Gibson and Klein before him at the time the invention was made, to modify the system of Gibson to include incrementing the value of the address counter because it was well known to monitor the data holding register to transition from accumulating data from the ROM to outputting data to the RAM (column 6, lines 25-27) as taught by Klein.

As per claims 5 and 19, the features specified in these claims as new features relating to program transfer means (consisting of all hardware means besides the CPU) would not be difficult to construct by a person skilled in the art.

As per claims 5 and 19, Klein discloses the loading logic circuit is contained in a field programmable gate array (FPGA) (RSC may be implemented in a programmable logic array; column 8, line 63 - column 9, line 1).

12. Claims 10 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gibson et al (WO 01/52062) and Fandrich et al (US 5,592,641).

As per claim 10, Gibson discloses the claimed invention as detailed above in the previous paragraphs. However, Gibson does not specifically teach a write protect mechanism that prevents the location of the storage device having the BIOS from being overwritten as recited in the claim.

Fandrich discloses a method and device for selectively enabling and disabling write access to flash blocks in a flash memory device, and a lock command locks (equivalent to the write protect) and unlocks a flash block in a flash array containing a plurality of flash blocks. Accordingly, it needs no creative efforts for those skilled in the art to realize the write protect mechanism for said logic circuit so as to prevent the location of the storage device having the BIOS from being overwritten (see abstract; column 1, lines 60-63).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the system of Gibson to include a write protect mechanism that prevents the location of the storage device having the BIOS from being overwritten because it was well known to protect the flash cell blocks from inadvertent program or erase operations (column 1, lines 62-63) as taught by Fandrich.

Claims 34-35 are rejected using the same rationale as for the rejection of claim 10 above.

13. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gibson et al (WO 01/52062) and Fandrich et al (US 5,592,641).

As per claim 11, As per claim 11, Gibson discloses the claimed invention as detailed above in the previous paragraphs. However, Gibson does not specifically teach a write protect mechanism generating write strobe signals as required in the claim.

MacDonald discloses a microprocessor performs a transfer (equivalent to the write strobe of a microprocessor) by programming the DMAC 25 and has Power-on values POV1 (equivalent to the first strobe signal), POV2 and POV3 (equivalent to the second strobe signal) (see page 5, line 31 to page 6, line 17).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the system of Gibson to include write strobe signals in the manner described by MacDonald because it was well known to protect the flash cell blocks from inadvertent program or erase operations (column 1, lines 62-63) as taught by Fandrich.

As per claim 12, MacDonald further discloses wherein value POV1 specifies the destination address for the power-up transfer (initial code in the storage device) (corresponding to that the first write strobe signal records the location of the BIOS in the storage device and the command code to the storage device); value POV2 provides a description of the non-volatile storage device for the power-up transfer and value POV3 specifies a transfer quantity that will allow the system to boot and it sets the corresponding field (corresponding to that the second write strobe signal enables writing of the storage device), and the DMAC 25 starts the transfer according to the values POVI, POV2 and POV3 (see page 5, line 31 to page 6, line 17).

As per claim 13, MacDonald further discloses the microprocessor CPU3 performs the transfer by programming the DMAC25 (it cannot directly overwrite the initial code in the storage device) (see page 5, line 31 to page 6, line 17).

REJECTION BASED on MacDonald:

14. Claims 1, 2, 8-9, 14, 16, 22-23, 26 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacDonald et al (GB 2,304,209) and Applicant's Admitted Prior Art (AAPA).

As per claim 1, MacDonald discloses a system for starting operation of an intelligent device comprising: discloses a system for starting a processor and specifically reveals the following technical features (see page 2, lines 9-20 of the description): a non-volatile storage device (equivalent to the application and file storage device) for storing at least initial operating code; volatile Random Access Memory (RAM); a Direct Memory Access Controller (DMAC) and a start-up logic circuit (corresponding to the loading logic circuit) coupled to the DMAC, the start-up logic circuit enabling the DMAC, and the DMAC being configured to access said non-volatile storage device and load at least part of the initial operating code in the volatile RAM.

However, it can be seen that claim 1 differs from MacDonald, in that, claim 1 generalizes an application and file storage device configured to read and write data files, one or more of the data files including the basic input/output system (BIOS) interface, while MacDonald does not have specific indication of a BIOS.

AAPA discloses that the BIOS is the initial operating code for initializing various hardware components (also described in page 1, lines 19-24 in the Background of the Invention, part of the description in the present application).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of MacDonald to include a BIOS as one of the data files because it was well known to provide an interface between the operating system and the hardware.

As per claim 2, MacDonald further discloses the following content: the DMAC being configured to access said non-volatile storage device and load at least part of the initial operating code (equivalent to the BIOS, see the comments on claim 1) in the volatile RAM; however, a microprocessor CPU is unnecessary for the process (see page 2, lines 15- 18 of the description).

As per claims 8 and 9, making both an original address on the non-volatile memory and a destination address on the RAM (POV1, POV2, POV3) settable transfer parameters could be easily inferred by a person skilled in the art from the invention described in MacDonald (see page 5, line 31 to page 6, line 17).

As per claim 14, MacDonald further discloses a method of starting a smart device comprising. MacDonald discloses the following technical features: Power-on circuit 1 sends a start-up signal to reset the microprocessor CPU3; the CPU3 is prevented from running until initial operating code has been sent to the volatile RAM8 (see page 5, lines 19-22 of the description for details); said initial code corresponds to the BIOS and is at least part of the code sent to the RAM (see the comments on claim 1 for details).

As per claim 16, MacDonald further discloses the following technical features: starting the CPU and accessing initial operating code in the volatile RAM (see page 2, lines 18-20 of the description).

Claim 22 is rejected using the same rationale as for the rejection of claims 1 and 2 above.

Claim 23 is rejected using the same rationale as for the rejection of claims 1 and 2 above.

Claim 26 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 31 is rejected using the same rationale as for the rejection of claims 1, 14 and 22 above.

15. Claims 3-4, 15, 20-21, 25 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacDonald et al (GB 2,304,209) and Applicant's Admitted Prior Art (AAPA) and Christeson et al (US 5,579,522).

As per claims 3, 20 and 32, MacDonald and AAPA disclose the claimed invention as detailed above in the previous paragraphs. However, MacDonald and AAPA do not specifically teach that the application and file storage device is a flash memory device as recited in the claim.

Christeson discloses a flash memory as an application and file storage device for storing and updating non-volatile code and/or data without the need for removing and/or replacing any computer system hardware components (col. 2, lines 36-39). Since the technology for implementing a flash memory was well known and since a flash memory benefits by storing and updating non-volatile code and/or data without the need for removing and/or replacing any computer system hardware components, an artisan would have been motivated to use a flash memory in the system of MacDonald and AAPA.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the system of MacDonald and AAPA to include a flash memory storage device because it was well known to benefit by storing and updating non-volatile code and/or data without the need for removing and/or replacing any computer system hardware components as taught by Christeson.

As per claims 4, 21, 25 and 33, MacDonald and AAPA disclose the claimed invention as detailed above in the previous paragraphs. MacDonald and AAPA do not specifically teach that the application and file storage device is a magnetic or optical disk drive as recited in the claim.

Christeson discloses a magnetic or optical disk drive as an application and file storage device for storing and updating non-volatile code and/or data without the need for removing and/or replacing any computer system hardware components (col. 4, lines 39-41; col. 2, lines 36-39). Since the technology for implementing a magnetic or optical disk was well known and since a magnetic or optical disk benefits by storing information and instructions without the need for removing and/or replacing any computer system hardware components, an artisan would have been motivated to use a magnetic or optical disk drive in the system of MacDonald and AAPA.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the system of MacDonald and AAPA to include a magnetic or optical disk drive storage device because it was well known to benefit by storing information and instructions without the need for removing and/or replacing any computer system hardware components as taught by Christeson.

As per claim 15, MacDonald and AAPA disclose the claimed invention as detailed above in the previous paragraphs. MacDonald and AAPA do not specifically

teach a user selecting which BIOS of multiple BIOS to copy into the RAM as recited in the claim.

Christeson discloses the following technical features: an additional BIOS region can be used to extend the system BIOS memory area. It can be seen that, the storage device can include multiple BIOSs and a user can select which BIOS to be copied into RAM (see col. 2, lines 41-55 of the description). Therefore, it is easy for those skilled in the art to obtain the technical solution of claim 15 based on the above combination of references.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the system of MacDonald and AAPA to include additional BIOS regions because it was well known to allow the processing logic of the computer system to update or modify any selected block of memory without affecting the contents of other blocks (column 2, lines 46-49) as taught by Christeson.

16. Claims 10-13 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacDonald et al (GB 2,304,209) and Applicant's Admitted Prior Art (AAPA) and Fandrich et al (US 5,592,641).

As per claim 10, MacDonald and AAPA disclose the claimed invention as detailed above in the previous paragraphs. However, MacDonald and AAPA do not

specifically teach a write protect mechanism that prevents the location of the storage device having the BIOS from being overwritten as recited in the claim.

Fandrich discloses a method and device for selectively enabling and disabling write access to flash blocks in a flash memory device, and a lock command locks (equivalent to the write protect) and unlocks a flash block in a flash array containing a plurality of flash blocks. Accordingly, it needs no creative efforts for those skilled in the art to realize the write protect mechanism for said logic circuit so as to prevent the location of the storage device having the BIOS from being overwritten (see abstract; column 1, lines 60-63).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the system of MacDonald and AAPA to include a write protect mechanism that prevents the location of the storage device having the BIOS from being overwritten because it was well known to protect the flash cell blocks from inadvertent program or erase operations (column 1, lines 62-63) as taught by Fandrich.

As per claim 11, MacDonald further discloses microprocessor performs a transfer (equivalent to the write strobe of a microprocessor) by programming the DMAC 25 and has Power-on values POV1 (equivalent to the first strobe signal), POV2 and POV3 (equivalent to the second strobe signal) (see page 5, line 31 to page 6, line 17).

As per claim 12, MacDonald further discloses wherein value POV1 specifies the destination address for the power-up transfer (initial code in the storage device) (corresponding to that the first write strobe signal records the location of the BIOS in the storage device and the command code to the storage device); value POV2 provides a description of the non-volatile storage device for the power-up transfer and value POV3 specifies a transfer quantity that will allow the system to boot and it sets the corresponding field (corresponding to that the second write strobe signal enables writing of the storage device), and the DMAC 25 starts the transfer according to the values POVI, POV2 and POV3 (see page 5, line 31 to page 6, line 17).

As per claim 13, MacDonald further discloses the microprocessor CPU3 performs the transfer by programming the DMAC25 (it cannot directly overwrite the initial code in the storage device) (see page 5, line 31 to page 6, line 17).

Claims 34-35 are rejected using the same rationale as for the rejection of claim 10 above.

NOTE: It is to be noted that the dependency of claim 35 on "claim 1" should be changed to "claim 31".

17. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacDonald et al (GB 2,304,209) and Applicant's Admitted Prior Art (AAPA) and Christeson et al (US 5,579,522) and further in view of Gefen et al. (US 2002/0138702).

As per claim 24, MacDonald and AAPA and Christeson disclose the claimed invention as detailed above in the previous paragraphs. However, MacDonald and AAPA and Christeson do not specifically teach that the storage device is a NAND flash memory device as recited in the claim.

Gefen discloses a storage device as a NAND flash memory device, which benefits from a lower cost, is non-executable and requires less routing resources (page 1, col. 0008). Since the technology for implementing a NAND flash memory was well known and since a NAND flash memory benefits from a lower cost, is non-executable and requires less routing resources, an artisan would have been motivated to implement a NAND flash in the system of MacDonald and AAPA and Christeson.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the system of MacDonald and AAPA and Christeson to include NAND flash memory device because it was well known to benefit from a lower cost, is non-executable and requires less routing resources as taught by Gefen.

18. Claims 5-7, 17-19, 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacDonald et al (GB 2,304,209) and Applicant's Admitted Prior Art (AAPA) and Klein (US 6,216,224).

As per claim 29, MacDonald and AAPA disclose the claimed invention as detailed above in the previous paragraphs. However, MacDonald and AAPA do not specifically teach incrementing the value of the address counter as recited in the claim.

Klein discloses a state machine drives the RSC to perform a number of operations that result in transfer of the ROM data to the RAM (equivalent to enabling the application and file storage device and the RAM); the address stored in the decrementing address counter 322 is used both to read data from the ROM and to write data to the RAM; the decrementing address counter 322 is decremented by one prior to the start of the first bus cycle of the next RSC operation (see col. 5, line 51 to col. 6, line 27 of the description for details). It can be seen that, the address counter is enabled to output a value and the value is correlated with a RAM address; while Klein discloses decrementing the value of the address counter. However, incrementing or decrementing the value of a counter belongs to the common sense for those skilled in the art and the corresponding incrementing or decrementing operation can be performed according to need.

Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of MacDonald and AAPA and Klein before him at the time the invention was

made, to modify the system of MacDonald and AAPA to include incrementing the value of the address counter because it was well known to monitor the data holding register to transition from accumulating data from the ROM to outputting data to the RAM (column 6, lines 25-27) as taught by Klein.

As per claims 5-7, 17-19 and 27, the features specified in these claims as new features relating to program transfer means (consisting of all hardware means besides the CPU) would not be difficult to construct by a person skilled in the art.

As per claim 5, Klein discloses the loading logic circuit is contained in a field programmable gate array (FPGA) (RSC may be implemented in a programmable logic array; col. 8, line 63 - col. 9, line 1).

As per claim 6, Klein discloses that the loading logic circuit is contained in a programmable logic device (RSC may be implemented in a programmable logic array; col. 8, line 63 - col. 9, line 1).

As per claim 7, Klein discloses the circuit comprises board level components (RSC may be implemented as application specific integrated circuitry or as hardwired logic circuitry; col. 8, lines 63-67).

As per claim 17, Klein discloses the step of copying the BIOS from a memory

storage device into RAM is controlled by a state machine (state machine transfers firmware routines from ROM to RAM; col. 4, lines 7-8).

As per claim 18, Klein discloses the state machine is implemented in an ASIC (col. 8, lines 65-66).

As per claim 19, Klein discloses the state machine is implemented in an FPGA (RSC may be implemented in a programmable logic array; col. 8, lines 63 - col. 9, line 1).

Claim 27 is rejected using the same rationale as for the rejection of claim 7 above.

19. Claims 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacDonald et al (GB 2,304,209) and Applicant's Admitted Prior Art (AAPA) and Le et al. (US 6,154,838).

As per claim 28, MacDonald and AAPA disclose the claimed invention as detailed above in the previous paragraphs. However, MacDonald and AAPA do not specifically teach copying additional interface device commands from the application and file storage device into RAM using the microprocessor as recited in the claim.

Le discloses copying additional interface device commands from the application and file storage device into RAM using the microprocessor to positively affect the economics of operating and maintaining the computer system (col. 14, lines 24-39).

Since the technology for implementing the copying of additional interface device commands from the application and file storage device into RAM using the microprocessor was well known and since copying additional interface device commands from the application and file storage device into RAM using the microprocessor benefits by positively affect the economics of operating and maintaining the computer system, an artisan would have been motivated to implement the copying of additional interface device commands from the application and file storage device into RAM using the microprocessor in the system of Le. Therefore, it is easy for those skilled in the art to obtain the technical solution of claim 28 based on the above combination of references.

Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of MacDonald and AAPA and Le before him at the time the invention was made, to modify the system of MacDonald and AAPA to include copying of additional interface device commands from the application and file storage device into RAM using the microprocessor because it was well known to positively affect the economics of operating and maintaining the computer system as taught by Le.

As per claim 30, MacDonald and AAPA disclose the claimed invention as detailed above in the previous paragraphs. However, MacDonald and AAPA do not specifically teach using error correction code as recited in the claim.

Le discloses using error correction code to positively affect the economics of operating and maintaining the computer system (col. 14, lines 24-39). Since the technology for implementing error correction code was well known and since an error correction code benefits by positively affecting the economics of operating and maintaining the computer system, an artisan would have been motivated to implement an error correction code in the system of Le. Therefore, it is easy for those skilled in the art to obtain the technical solution of claim 30 based on the above combination of references.

Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of MacDonald and AAPA and Le before him at the time the invention was made, to modify the system of MacDonald and AAPA to include an error correction code because it was well known to positively affect the economics of operating and maintaining the computer system as taught by Le.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach copying BIOS from application and file storage device into RAM without using a microprocessor and write protect a location having BIOS from overwrite.

21. The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

22. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (571) 272-4215. The examiner can normally be reached on 8:30 am - 6:00 pm, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 19, 2006

Pierre Vital

PIERRE VITAL
PRIMARY EXAMINER